Method for realization of self-controlling loop apparatus structures

Dimitar Tyanev, Dragomir Yanev, Stamen Kolev
Technical University, Varna, Bulgaria

Abstract: *This paper presents a novel methodology for design of operational computational devices, realizing a diversity of condition-controlled loop algorithmic structures. The synthesis of such a structure takes in count just the necessary for the computation signal changes, which makes the synthesis of controlling finite state machine unnecessary. Thus the resulting controlling circuit is tightly coupled with the logic one. In this sense the structure can be defined as self-controlling and can be part of micro-pipeline structure with certain delay. The structures in either case are as fast as possible. Experiments have been made with Xilinx' FPGA chip.*

Keywords: *Computational devices, Micro-pipeline, Controlling automata.*

1. INTRODUCTION

Nowadays the realization of the computational process goes deeper in the lower hardware levels. Opportunity for that is the potential of developed programmable elements [12]. There are no popular formal methodologies for the implementation of an arbitrary computational algorithm on hardware. A reason for this is the difference in hardware and software design. Authors take advantage of programmable hardware technologies and propose such a methodology.

Authors' goal is defined in their previous papers [1, 2, 3, 4]. Basically the idea is to develop methodology for hardware realization of arbitrary computational algorithm, which is free of micro-program controlling device, having a novel form of organization and characteristics.

A methodology for hardware realization of one of the basic algorithmic structures, the condition-controlled loop, is presented in the present work. The block diagram of the loop is depicted below (figure 1.1).

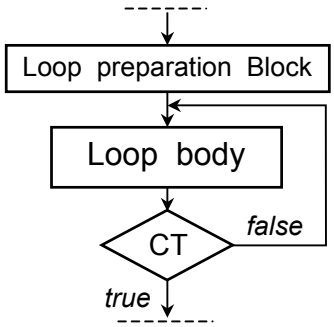


Figure. 1.1 Condition-controlled loop block diagram (CT – Condition test)

Typical for the structure is that the loop body is executed until certain condition is changed. The condition is re-evaluated and tested at each iteration of the loop. Usually the condition has the following form:

$$(\Delta Var)_k < \varepsilon \quad , \tag{1.1}$$

where $(\Delta Var)_k$ is the k-th change in the control value Var, and ε is the a priori known accuracy. Represented condition is synthesized on the basis of initial technical information for the task, so the calculations related to the condition test (CT) will be part of the operational combinational circuit in the structure of loop section.

2. TWO REGISTER SELF-CONTROLLING LOGIC STRUCTURE

In their nature loops are evaluations of the same operations on changing data. Since the hardware implementation of these operations with common operational combinational circuit is usually complex, the structural development in the form of flatterned loop is very inefficient solution. Therefore, here it is proposed to be implemented once. This decision leads to the need loop structure to be synthesized as closed feedback with temporary memory cells.

The temporary memory is represented by the register R2, which is synchronous edge-trigged, working at rising edge. To hold the input data stable is used latch type register R1. As a result of these considerations is synthesized two register structure with distributed logic [6] presented in figure 2.1

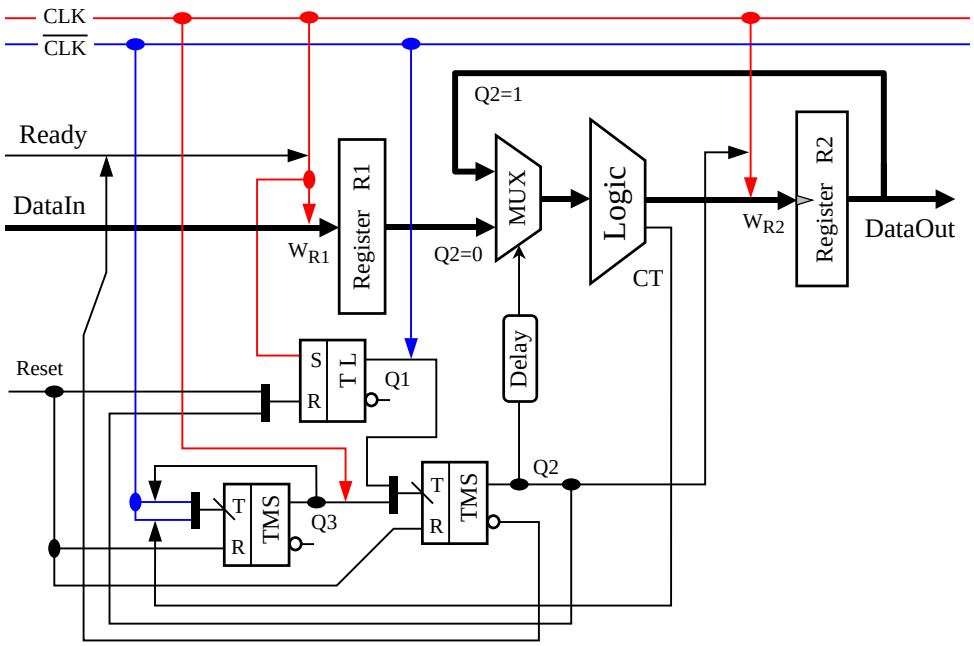


Figure. 2.1 Condition-controlled loop – operational structure

Register R2 holds temporary results while proceeding and at the end – the final result. This version of the hardware implementation of the algorithmic structure is proposed as a method of self-controlling loops implementation. It is in full compliance with the basic concept of the study as it is free of micro-program controlling device.

The loop calculation is clocked in the loop of register R2 and operational combinational circuit, which is formed by maintaining the state of multiplexer MUX. Multiplexer switching is delayed by propagation delay time of element “Delay”. The purpose of this delay is to achieve a reliable fixation of the results in register R2 at the initial state of loop’s calculation. Such a delay of the signal can be realized by even number of inverters included consecutively.

Concurrently with the temporary results, condition test circuit calculates the termination condition. The value of condition test is used to manage the termination of the synchronous switching and setting the structure in the initial state.

Operating of the structure is controled by the internal logic circuit, consisting of three flip-flops. Logic signals are as follows:

1. Strobe pulse – write input data:

$$W_{R1} = \text{Ready} \cap \overline{Q2} \cap \text{CLK} \qquad (2.1)$$

2. Strobe pulse – write data in $\Phi 2$

$$W_{R2} = Q2 \cap CLK \tag{2.2}$$

3. Control signals for Latch trigger Q1:

$$\begin{aligned} S &= W_{R1}\,; \\ R &= Reset \cup Q2\,. \end{aligned} \tag{2.3}$$

4. Flip-flop Q2 working at falling clock edge with the following control signals:

$$\begin{aligned} T &= (Q1 \cap \overline{CLK}) \cup (Q3 \cap CLK)\,; \\ R &= Reset\,. \end{aligned} \tag{2.4}$$

5. Flip-flop Q3 working at falling clock edge with the following control signals:

$$\begin{aligned} T &= (Q3 \cap \overline{CLK}) \cup (CT \cap \overline{CLK})\,; \\ R &= Reset\,. \end{aligned} \tag{2.5}$$

6. MUX is switched by selection signal Q2 as follows:

$$\begin{cases} MUX \to R1, & \text{when } Q2 = 0; \\ MUX \to R2, & \text{when } Q2 = 1. \end{cases} \tag{2.6}$$

Intermediate results are recorded in the register R2 on rising edge of clock signal CLK. So in the feedback circuit (see figure 2.1) is done continuous clocked calculation until the test condition terminates the loop CT=1.

In the clock cycle, which will be the last one, some of the results are set appropriately so the system detects the test condition as true. This value is used to generate a sequence of pulses that drive switching flip-flops control circuit. These pulses terminates the calculations and establishes initial state, which can be hold indefinitely. The whole switching procedure is shown on figure. 2.2.

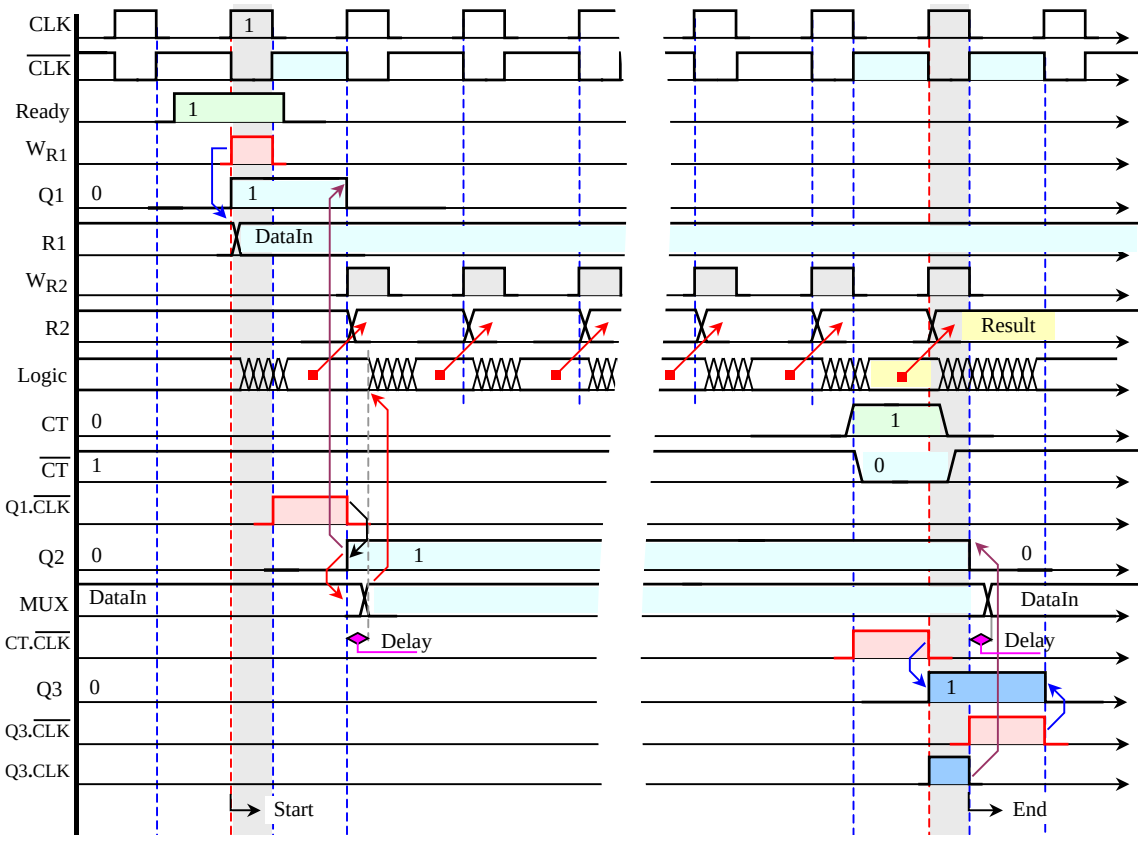


Figure 2.2 Full loop's timing characteristic

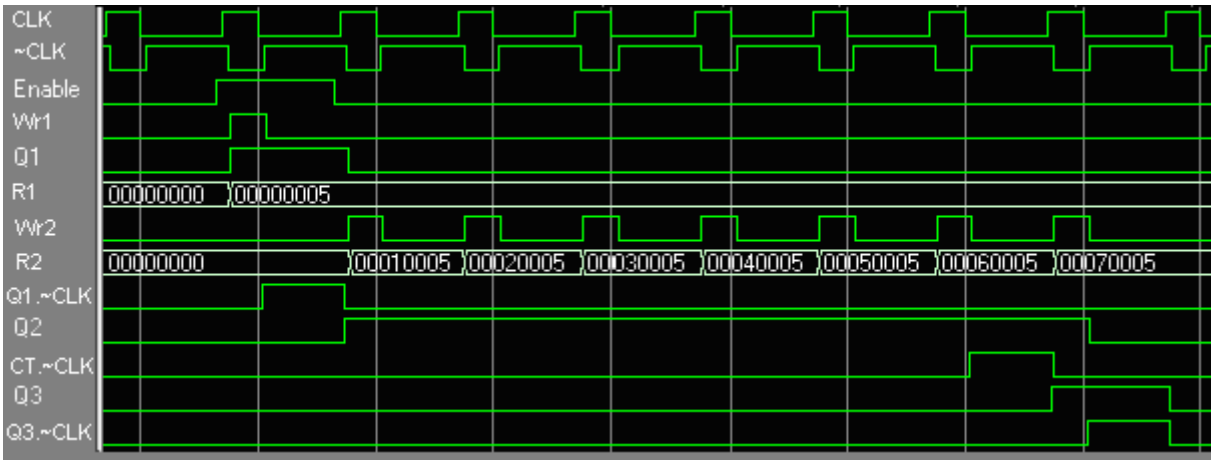
New computational process starts with the appearance of sgnal Ready (permission) that must satisfy the following two requirements – to appear on the falling edge of clock signal and to have a duration not more than one clock period.

The circuit can be set to initial state on Reset or CT signal

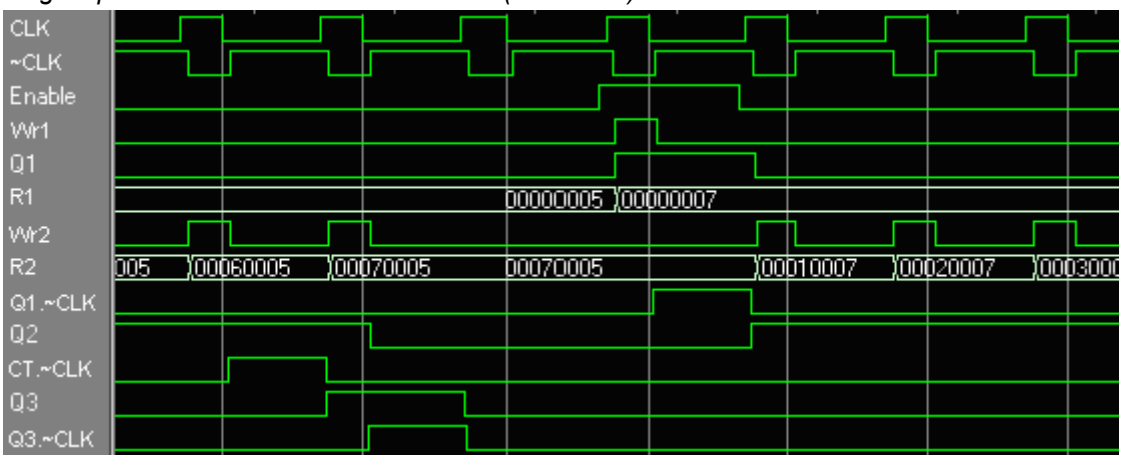
3. EXPERIMENT

The possibility for practical realization of the proposed, in this work, thesis was experimented using programmable logic. It was used *Xilinx* ISE 10.1 development environment. The structure was coded in VHDL and Xilinx Spartan 3 device was used. For the simulation ModelSimXE III 6.2g is used. The corresponding model behavior is shown on figure 3.1. The identical behavior of the proposed structure and the simulated model proves the stated thesis of the research.

Executing loop until condition test becomes true



Executing loop until condition test becomes true(continued)



Finishing the loop and starting new one with different input data

Figure 3.1 Testbench waveform of the project

CONCLUSIONS

As with the structures, which were object of the previous authors' research works, the main complication appeared to be the use of one phase clock generator. The authors believe that the use of multi phase generators will simplify the design of the structure and especially the controlling circuit.

The presented in this paper research complies with the results published by the authors earlier. These results prove the possibility for hardware realization of self-

controlled computational structures, free of controlling finite state machine. That makes the authors more confident in their belief that the hardware realization of any arbitrary algorithm as self-controlling is possible. Yet there are algorithmic structures, which are not investigated in the sense of the main authors' idea.

REFERENCES:

[1]. Josiffov V., Kolev St., Tyanev D., *Operational structures without controlling automata*, International workshop on network and grid infrastructures, Institute for parallel processing at the bulgarian academy of sciences department "distributed computing systems and networks", Sofia, Bulgaria, 27-28 Sept. 2007, EC Project BIS21++ "Bulgarian IST centre of competence in 21 century",

[2]. Тянев Д. С., Колев С. И., Йосифов В., *Метод за реализация на апаратни самоуправляващи се циклически структури*, Годишник на ТУ-Варна, Юбилеен сборник "45 години ТУ-Варна", 2007, ISSN 1311-896X, стр. 130-135,

[3]. Kolev St., Jossifov V., Master thesis: "*Design of asynchronous pipelines for floating point multiplication and division",* FHTW – Berlin, Deutschland, 2007.

[4]. Тянев Д. С., Колев С. И., Янев Д. В., *Метод за реализация на апаратни самоуправляващи се циклически структури – част II*, Списание "Компютърни науки и технологии", V, брой №2/2007, ISSN 1312-3335, 23-30.

[5]. Тянев Д. С., *Организация на компютъра*, Том 1, ISBN 978-954-20-0412-7, Издателство на Технически университет - Варна, 2008, www.tyanev.com

[6]. Тянев Д. С., *Организация на компютъра – упражнения*, ISBN 954-20-0258-0, Издателство на Технически университет - Варна, 2007 год., www.tyanev.com

[7]. Тянев Д. С., *Организация на компютъра – проектиране на логически структури*, ISBN 954-20-0259-9, Издателство на Технически университет - Варна, 2004 , www.tyanev.com

[8]. Patterson D. A., Hennessy J. L., *Computer Organization And Design*, Morgan Kaufmann Publishers, ISBN 1-55860-604-1, 2005.

[9]. Sutherland I. E., *Micropipelines*, Communications of the ACM, June 1989 Volume 32, Number 6.

[10]. John F. Wakerly, *Digital Design – principles and practices,* Fourth Edition, Prentice Hall, ISBN 0-13-186389-4, 2005.

[11]. Булгаков С., Мещеряков В., Новоселов В., Шумилов Л., *Проектирование цифровых систем на комплектах микропрограммируемых БИС*, Москва, "Радио и связь", 1984.

[12]. WEB-адрес на фирма XILINX – http://www.xilinx.com/

[13]. Pong P. Chu, *RTL hardware design using VHDL*, Wiley - IEEE Press., ISBN 0471720925.

[14]. Yau-Hwang Kuo, Shaw-Pyng Lo, *Partitioning and Scheduling of Asynchronous Pipelines*, Institute of Information Engineering, National Cheng Kung University, Tainan, Taiwan., Proc. of CompEuro'92, The Netherlands, May, 1992.