OPERATIONAL STRUCTURES WITHOUT CONTROLLING AUTOMATA

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Abstract: *This document presents a new method for design of operational computational devices, in a way that a FSM is removed from the design. The method can be used for the design of synchronous and asynchronous devices. The main advantages of the method are the simplification and homogenization of the devices and as well the opportunity of increasing the output of the computational devices.*

Nowadays, the design flow of digital computational apparatus is significantly different than the one in recent past. The reason for that are the evolution of the programming tools for automation of the design flow and the greater possibilities that their building blocks give. Due to the evolution of the technology, in general, is possible the realization of methods and approaches for design like the one proposed by the authors. The biggest advantage of the method appears to be the possibility of direct apparatus realization of some forms of parallelism in the logical computations.

1. Traditional concept

Let us consider the traditional structure of computational device depicted in figure 1.
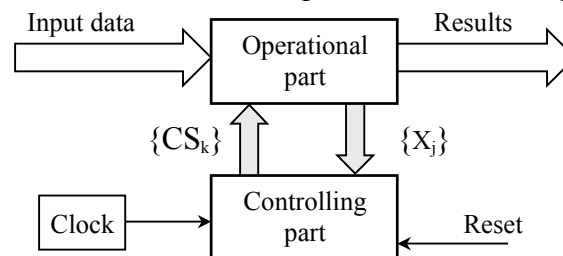

Fig. 1 Traditional device structure

The functioning of the represented structure can be organized by the synchronous or asynchronous control method, or by combination of both. In the case of the asynchronous control, the clock generator is absent and additional signals of "end of micro-operation" {End's} appear as shown on figure 2.
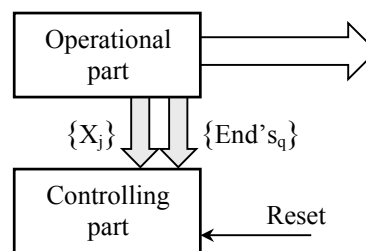

Fig. 2 Additional signaling in the asynchronous control

Typical for the traditional control organization is, that the control device in the computational structure realizes the controlling algorithm in micro-operational level as finite state machine.

The purpose of our research is to show, that the basic algorithmic structures (linear parts, conditions and loops), which can fully describe the control algorithm realized by the control device, can be transferred (embedded) in the operational device. When achieving our goal, in the computational structure remains only the modified operational device, which is result corresponding to the modification of the controlling device. Our understanding for the final result is presented in figure 3.
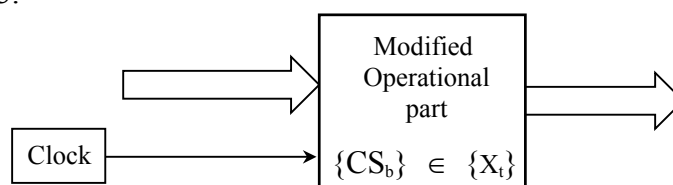

Fig. 3 Device without controlling automata

The main effect of the opportunity of achieving our goal is the removal of the separately existing controlling device and its transformation in forms, which after applying rules discussed further in this material, are integrated in the operational device.

2. Realization of the main algorithmic structures

Proceeding from theoretical assumption, that the controlling part of the computational device is synthesized in absolute conformity with the algorithm of its functioning, the main objects of our research are the basic algorithmic structures, which can be met in an algorithm.

Linear/sequential algorithmic structure

The linear algorithmic structure, represented in picture 4, is organized as unconditional transfer of control and is a sequence of micro-commands, which are executed consecutively in the operational part of the computational device under the control flow of the consecutively sent control signals.
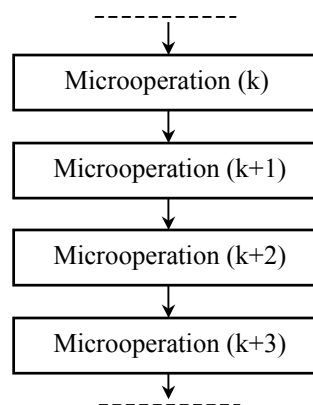

Fig. 4 Sequential algorithmic structure

Our concept for the functioning of the control part is expressed with anticipation of consecutive switching over its internal states caused by sequence of clock pulses or signals of the type "end of operation". The traditional organization can be represented in following way:

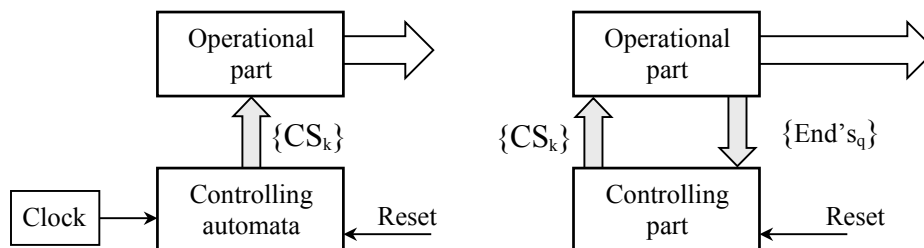

Fig. 5 Possible organizations of the computational process

Which makes clear, that main engine of the computational process is ether the clock generator or the signals of type "end of operation" $\{End's_q\}$.

The functioning of the FSM in the structure depicted in figure 5 is a process of switching between the states of the FSM in which in different points of the operational part are applied different control signals. The output of the control device is set of control lines. As to the input, it is one line as it comes to the synchronous method for control and as to the asynchronous method for control the output is set of "end of switching" lines. The flow of the computational process in time is shown in the following time-diagram (fig. 6).
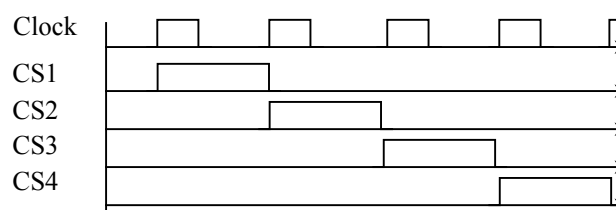

Fig. 6 Time-diagram of the process of controlling sequential structure

In the guide line of our concept, we can claim, that the controlling device is a kind of multiplexer, which distributes the different clock controlling signals and applies them in different parts of the operational part. Our assumption for the controlling automat is as distributor for the clock pulses which appear in different parts of the operational device, but in one and only way (in the time as depicted in figure 6).

Deriving from that concept we reach to the conclusion, that the controlling automat can be removed from the computational structure by appropriate modification of the operational device. The core of the modification goes through the pipelining of the operational part. We will clarify this statement with the help of figure 7, which represents sequence of four control signals. These four signals lead to the execution four different micro-operations and these four different micro-operations are realized by four different operational circuits. They are consecutively placed and form four stage pipeline as shown on figure 7.
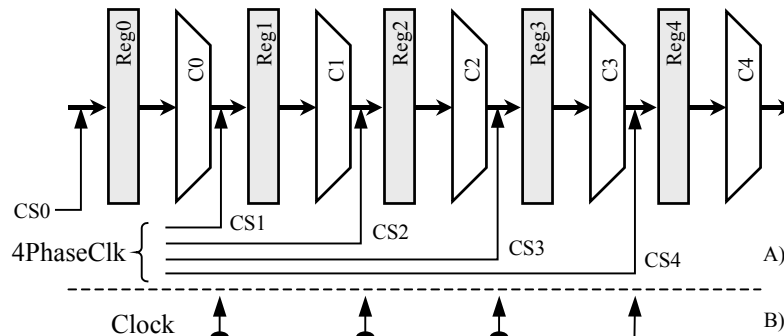

Fig. 7 Pipeline organization of the sequential structure

The control of the pipeline simply requires suitable clock pulse sequence. It can be realized as common one-phase clock generator (variant A fig. 7) or as multi-phase (four phase) clock generator (variant B fig. 7). The solution, in the terms of our goal (removing the controlling device (look at picture 5)), which naturally derives, is to remove the additional registers from the pipeline structure, which results in one computational circuit as depicted in figure 8.
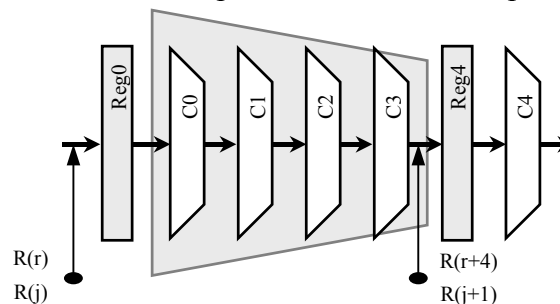

Fig. 8 One phase computation transition

The removal of the intermediate registers from the pipeline structure (that is our modification in linear structure) leads to one-phase computation of the group of micro-operations.

Conditional algorithmic structure

The conditional algorithmic structure is defined by the conditional branching as shown on picture 9. The branching is controlled by the generated in the operational part condition (signal X_j), which in the traditional structure is checked in the controlling device (look at figure 1).
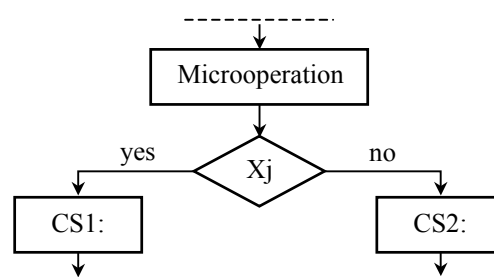

Fig. 9 Conditional algorithmic structure

Externally for the operational device, what indeed the controlling device does is to choose between two controlling signal CS1 and CS2. This is depicted in figure 10 in its left part.

Fig. 10 Removing the controlling automata

The problem for removing the control as part of the controlling device in this case we solve as shown on figure 10 in its right part. The algorithmic choice, which the controlling device should make, can be easily realized out of the controlling device in a single circuit, which generates the controlling signals as values of the function of the, returned from the computational part, signals. This possibility leads us to the conclusion, that the control is took away from the controlling device (as shown on figure 10), with which we claim that we have achieved our goal in the case of conditional branching.

The functionality of the resulting circuit is defined and concretized depending on the following algorithmic progress of the two branches of the conditional structure. We may have versatile cases in the algorithmic structure beyond the conditional part, which will affect in different manner the considered structure depending on the different algorithmic jumps [lit. Po OK]. These cases are minimized to several, which we will analyze.

The main structure, shown on figure 9, defines the functionality of the resulting circuit as demultiplexer, which makes the choice between the controlling signals. In picture 11 we consider one of the main possible cases of the algorithm progress, where we can have two parallel linear parts, joining in one common point.
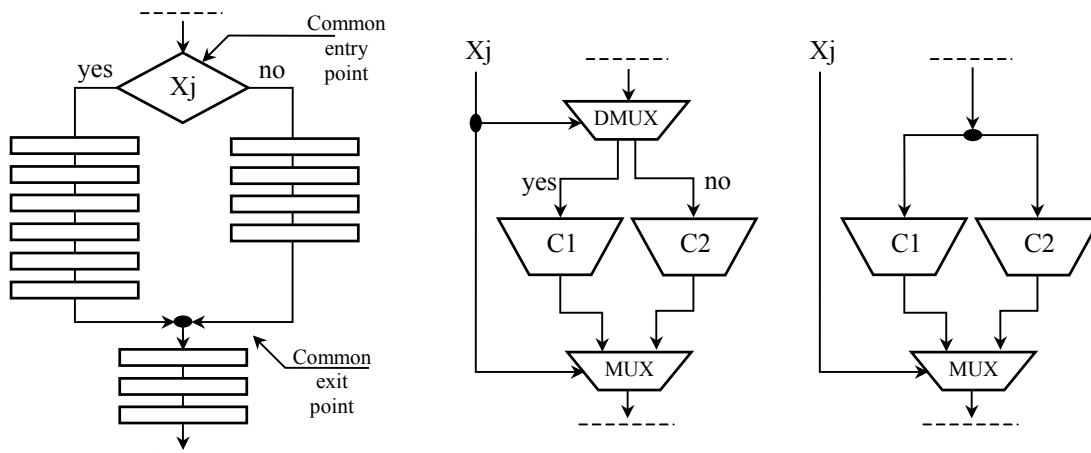

Fig. 11 Self control scheme

In this case, to achieve our goal, we offer two solutions. The resulting structure consists of two parallel sequential circuits C1 and C2, as discussed in point 1. These two parallel structures have one common input point and one common output point. Thus the conditional structure can be realized in two distinct ways according to our comprehensions for the functioning of the parallel structures:

А) The input point has the functionality of demultiplexer, in which the input data is passed only to the chosen parallel circuit, which calculates the true result. The other parallel circuit logically is not functioning (Figure 11 the middle picture). Then the output point has the functionality of multiplexer, through which passes the result, calculated in chosen branch. The choice in the demultiplexer and in the multiplexer is made according to the condition X_j ;

Б) The input point is common for both the circuits C1 and C2, which means, that they both receive the data, operate simultaneously and both have results at their output (figure 11, the right picture). The output point has the functionality of multiplexer with argument X_j, according to which the choice is made.

The complexity of the conditional structure may vary if additional conditions are present but in general the complete conditional structure has one common entry point and one common exit point. In its body it may contain various number of conditional sub structures but in all of these cases, for achieving our goal, it is possible to apply the solution, depicted in figure 11, that is why consider the solution for common.

The analysis of the computational process shows, that in a lot of cases there is a group of repeating calculations. That fact brings us to the idea for the short algorithmic representation of these repeating calculations by organizing the repetitions with the help of condition, which is called "end of the repetition condition". The condition is formed according to the nature of the repetition, for which we can say, that their number can be preliminarily known or preliminarily unknown. The special use of the conditional structure in that case leads us to the known loop structure.

The loop structure

Two kind of loops are known:
1. Count-controlled loops ;
2. Condition-controlled loops.

For the formal organization of structures of the first type is used the fact, that their count is preliminarily known and is controlled by variable called counter. The condition for the end of the loop is determined according to the value of the counter. The common loop algorithmic structure is shown on figure 12.
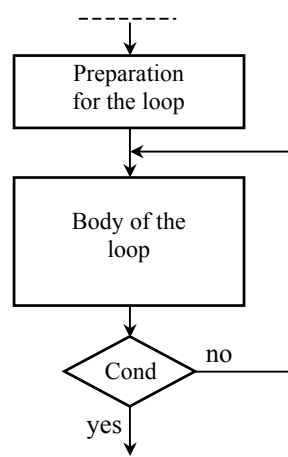

Fig. 12 Loop structure

The traditional control of the operational part of the computational device executing a count-controlled loop, needs hardware realization of the counter. The signal showing the end of the loop is formed by decoding the output of the counter and is analyzed in the controlling part, results in exiting or not the loop.

The algorithmic organization of the repetition may be achieved without the formal condition, without using conditional algorithmic jump, simply by pure repetition of the group in the body. Such kind of organization of the repetitions results in sequential algorithmic structure (figure 13), which we already described.

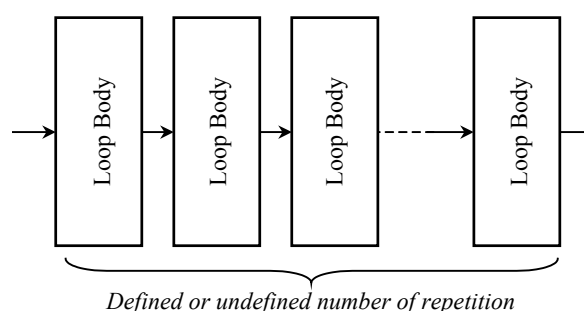*Defined or undefined number of repetition*

Fig. 13 Loop body repetition

The removal of the control, as part of the controlling device, in this case we propose to be done by the pure repetition of the computing circuit representing the loop body as already shown in figure 13. Such a solution reorganizes the loop structure in sequential the control of which we already presented.

For the formal organization of the condition-controlled loops is necessary to be synthesized condition for the end of the operations. This condition usually formed according to the nature of the computation. Commonly the condition is related with the achievement of given precision or matching given value. The repetition in the conditional-controlled loops can not be organized by repeating the circuit of the loop body as shown in figure 13.

After the said for the two kind of loops we reach to the conclusion, that, as for the loop structure, we have achieved our goal partially. The practical realization of a loop with the verification of any kind of condition leads to operational structure with feedback. The research of feedback structures with control without controlling automata requires special attention and will be presented in another ours publication.

3. Conclusion

We can conclude, that the expressed, by an algorithm, computational process can be realized in a computational device, the logical structure of which differs from the traditional structure, i.e. it does not contain controlling device as depicted in figure 3. In deed the modified operational device is one phase circuit or pipeline of intermediate registers are used.

From methodical point of view, the presented method for synthesis of computational devices, is based on the synthesized for its functioning algorithm. To extract the described main algorithmic structures, this algorithm is decomposed and thus we can apply the obtained solutions. In general the resulting structure of the operational device is a kind of concatenation of the separate solutions.

The main advantage of the method consists of the possibility for quick reduction of the count of the sequential pulses by the time of the algorithm execution. That includes reduction to one phase too. The throughput can be increased more by applying pipeline organization in the sequential parts.

The main disadvantage of the method is, that increases the volume of circuitry compared to those when traditional control structure is used.

In coming publications, the authors will present samples for the application of the method.

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