ORGANIZATION OF DMA-TRANSFER FOR ISA-BASED A/D CONTROLLERS

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Abstract: *The object of discussion in this study are the foremost means for data input through the channels for direct memory access by ISA-based controllers, intended for synchronic and asynchronic analog-digital conversion. The requirements of the process of transfer needed for synthesis are also clarified. The potential technical and program solutions are based on two of the DMA-controller operation modes - single transfer mode and block transfer mode.*

Key words: DMA-controller, A/D-controller.

1. Direct memory access

In order to examine an actual process, the computer system needs its digital projection. The possibility for this projection to be obtained is ensured by hardware and software devices of a system for data input. These devices are not common for the computer configurations spread on a large scale. The requirement for simplicity in structure and control of this system leads to research of analog-digital controller (A/D-controller), based on the system computer bus, for example one belonging to the ISA-standard. The deprivation of the user's A/D-controller of its own memory means that it will use the available main storage, the access to which will be periodical in the cyclical repetition of both operations conversion and input. Under these circumstances and taking into consideration the high requirements to the stability of frequency of discretization of the analog signal, which can be achieved by the use of quartz stabilisation, we become aware of the fact that the control of the analog-digital conversion and data reading from the A/D-controller is advisable to be obtained by the DMA-controller signals. Usually the computer platforms offer user-free DMA-channels for 8-bit transfer and DMA-channels for 16-bit transfer. Most suitable for realisation of data transfer from the A/D-controller to the main storage are two of the modes of DMA-channel - single transfer mode and block transfer mode.

A) Single transfer mode

When the DMA-channel is programmed to operate in this mode (bits b7 and b6 in the mode register have values b7=0, b6=1), the transfer of every single account received in the A/D-controller to the main storage is being fulfilled by the controller initiative. It achieves this by applying a request for service to the DMA-controller. In response the DMA-controller wants form the processor the right to operate the system bus and after it has attained that right, it performs transfer to the corresponding cell in the main storage of A/D-controller-shaped account. This exhausts the duties of the DMA-controller, it discharges the system bus and remains in stand-by position. The processes of conversion and transfer in this mode of DMA-channel are shown on Fig.1.

By the timing-diagram we can reach the conclusion that the speed of the analog-digital conversion is set by the tact signal ***Start ADC***. Every negative front of this signal starts a new conversion during which the accounts of the amplitudes follow with a time step **T**. Within the **T**-period three stages are observed in the process development. The first stage, with duration **T1**, belongs to the analog-digital converter and is determined by its speed possibilities. The **T1** interval starts from the negative front of the tact signal ***Start ADC*** and ends with the negative front of the **Ready** signal, which appears in the converter when all digits of the account are ready. This time interval is constant and cannot be operated, as it represents a technical feature of the converter itself.

The second stage, with duration **T2**, belongs to the DMA-controller and is determined by the duration of the machine cycle on the system bus. Its beginning coincides with the moment of initiation of the ***Ready*** signal and it ends with the data write in the memory. In this temporary interval the following procedure is performed: the converter gives ***Ready*** signal indicating prepared data and is used by the relevant logical circuits for ***DREQ*** transfer, which request is lodged in to the corresponding DMA-channel. The ***DREQ*** signal initiates in the DMA-controller attempts for occupation of the system bus and data transfer from A/D-controller to the main storage. After completion of transfer, the DMA-controller removes the confirming signal ***DACK***, the ascending front of which marks the end of this stage. The transfer time **T2** of the current account is a little longer than a machine cycle and cannot be altered.

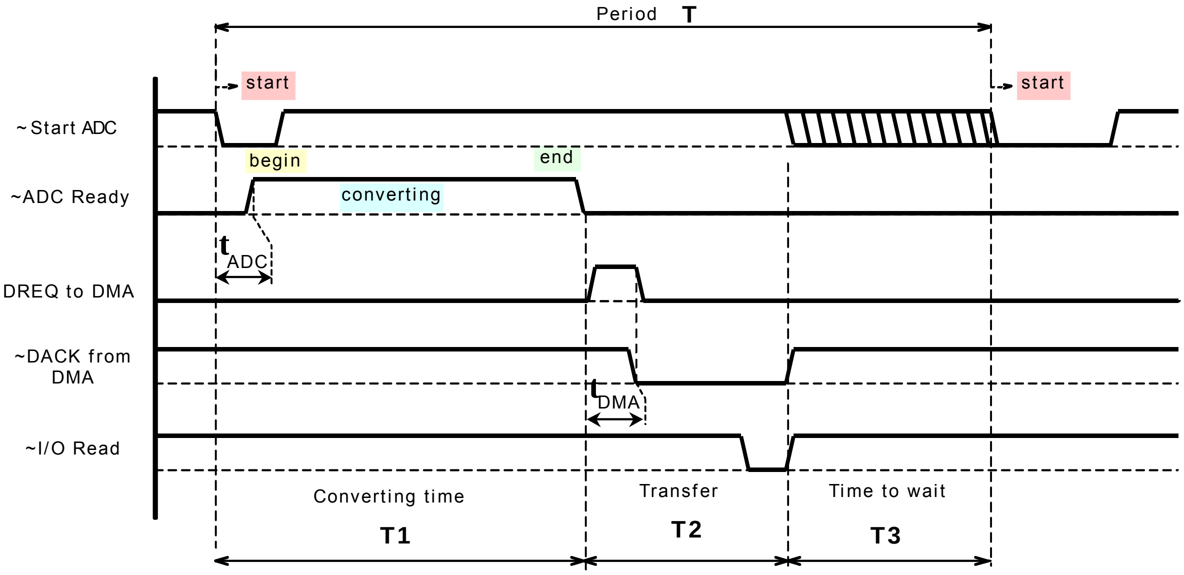

Fig. 1

The third stage, with duration **T3** can be concisely expressed as stand-by time. In this temporary interval both A/D controller and the DMA-channel are in stand-by position. The first expects a starting front in the ***Start ADC*** signal, the latter - a request ***DREQ***.

Various technical solutions using the above-described procedure for data transfer by the means of DMA-channel, operating in the single transfer mode, are described in [1], [2], [3], [4].

It is worth to regard also the speed possibilities of a system for data collection, using this method for transfer organization, as they determine its application. The low rates of the analog-digital conversion are reached by extending of the period **T** of the starting impulses. Usually the speed alteration is realised by program-operated divisor of the tact frequency. It can be supposed that the realization of low rates of discretization does not have any theoretical or organizational limits. But this is not the case with the high rates.

There are two possibilities for achieving top rates of discretization and transfer in the method of transfer organization we're examining. The first one can be reached by increasing the starting signal frequency, which is conveyed by decreasing the temporary interval **T3**. Theoretically speaking, this interval could be removed, i.e., **T3=0**, but practically it's dangerous to do this. The risk comes form the fact that the end of the temporary interval **T2** is not always at one and the same distance from the beginning of the period **T**. In the first place that is due to the asynchrony between the tact impulses of the ***Start ADC*** signal and the tact impulses of the converter itself. This asynchrony enters the variable delay $\mathbf{t}_{ADC}$ (see Fig.1). Secondly, the time for which the DMA-controller occupies the system bus $\mathbf{t}_{DMA}$ (see Fig.1), is also variable. As a result there exists a possibility that in some of the A/D-controller cycles appear starting of the converter before the transfer of the current account is over, i.e., (**T1+T2**)>**T**.

The second possibility consists in choosing the appropriate analog-digital converter. The faster it receives the accounts, the shorter the temporary interval **T1** is. It can be assumed theoretically that this interval vanishes to a zero. Thus it comes out that the speed limit of the analog-digital conversion is determined only by the throughput of the system bus. Anyway, having in mind the peculiarities of the considered transfer mode with which in the operation of the system bus the processor and the DMA-controller take turns, one comes to the conclusion that the minimum value to which the period **T** of the starting impulses can aim at, is two machine cycles which according to the

ISA standard comes up to 2 [μs]. When using the DMA-channel for 16-bit transfer that means collection of accounts with speed close to 10^6 [B/s].

If the analog-digital converter has output register for data storage, i.e., if it can combine in time the procedures of conversion and data reading, then when the negative front of the signal ***Start ADC***, initiating the converter, can be shifted at certain conditions even more to the left from the end of the temporary interval **T2**, as shown on Fig.2.

The condition needed for operating the way it is shown on Fig.2 is: **T1>T2**. It means that the described methods for this operation mode for control of the A/D-controller, are worthless to be applied unless in case used converter has conversion time not shorter than 1 [μs].

B) Block transfer mode

When DMA-channel is programmed for operation in this mode (bits b7,b6 in the mode register have values b7=1, b6=0), the transfer of the requested number of accounts is performed through continuously consecutive transfer cycles, initiated by one single request. After occupying the system bus, the DMA-controller does not discharge it until the flag **TC** (Terminal Count) is formed. With this operation mode (continuously consecutive pure cycles of transfer), the DMA-controller counts on the constant readiness of data source for reading. Here it means that every single account, has to be received by the A/D-controller, within one machine cycle.

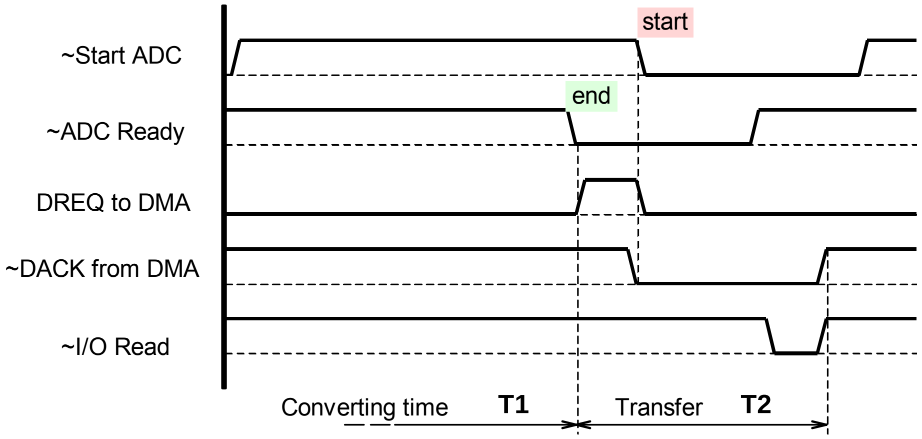

Fig. 2

The speed parametres of conversion, the requirements to the hardware part of the controller, as well as the algorithms of its control; are best explained on the block-scheme of the microprogram control of the DMA-controller [5], [6]. Figure 3 shows a general graph of its states when working in the block mode.

It's obvious that if the condition for end of the transfer cycle (**TC**=0) is not acknowledged, the DMA-controller consecutively goes through four transition stages (S1, S2, S3, S4), and sends the needed control signals to the processor, to the memory and to the peripheral device. Not in every cycle, though, these states are present simultaneously. Usually the carry of the eighth bit of the address equals to zero (p7=0), which means that when there's a normal timing diagram, the states (S2, S3, S4), (S2, S3, S4)... are consecutively following each other. The normal timing diagram is carried out when bits b0 and b3 in the control register of the DMA-controller form the conjunction $\overline{b0} \wedge b3 = 0$. With every 256 such cycles (see Fig.3) emerges the carry **p7** (p7=1) and then a branch transfer is carried out and through the S1 state - .... (S2, S3, S4), (S1, S2, S3, S4), (S2, S3, S4) ,.... As the target of interest here is the top speed for operation of the A/D-controller which is due to receive every account within an single cycle of the DMA-controller, as a consequence from the above-mentioned facts the typical time for this is a bit shorter than three system tacts, i.e., T1>3*210=630 [ns].

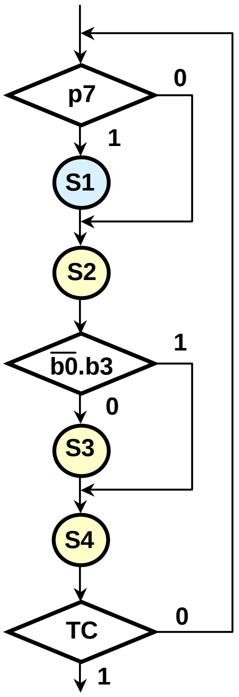

Fig. 3

In order to provide this operation mode each data reading from the A/D-controller is due to perform a start of the following conversion. The most appropriate signal for that purpose is ***I/O Read***. Figure 4 shows a process of multiple data reading by the A/D controller when the DMA-channel which handles it, operates in a block transfer mode. It's taken into account also that the converter combines the processes of conversion and storage of the preceding account in time.

Though the **Si**-states of the DMA-controller are interchanged synchronically by quartz-stabilized tact impulses, this discretization will be defined by us as asynchronic. The user needs to know that the temporary step between two adjacent accounts, stored in two adjacent memory cells, not always remains the same - at every 256 steps each consisting of 630 [ns] comes a single step consisting of 810 [ns]. It applies to accounts which are to be found in cells which addresses in their low byte change from value **xx...xxFF** into value **yy...yy00**. In case that for writing of the real process the user can be contented only with those 256 accounts then when there's a suitable initial address (**xx...xx00**), one will receive then with an absolutely synchronic process. If one ignores the appearance of state S1 in the machine cycle of every 256 cycles each consisting of 3 tacts, it can be assumed that when using 16-bit DMA-channel, operating in block transfer mode, the accumulation of accounts with speed close to $3{,}17 * 10^{6}$ [B/s] is possible.

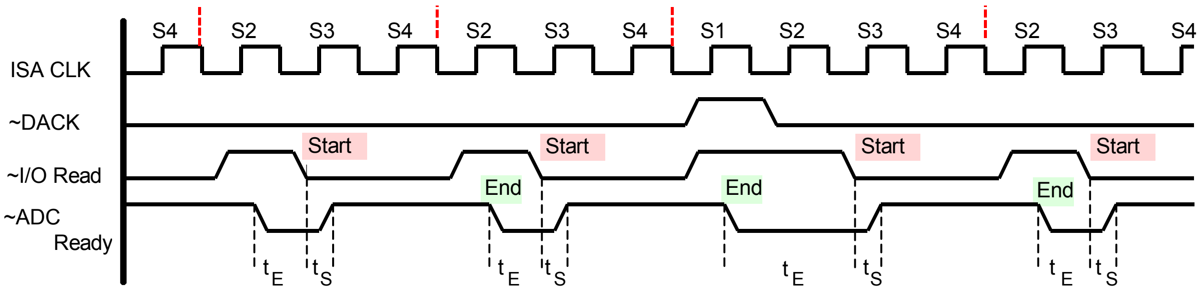

Fig. 4

When the DMA-channel is programmed for performing compressed timing-diagram ($\overline{b0} \wedge b3 = 1$), then state S3 is excluded from the transfer cycles (see Fig.3). Then the DMA-controller performs its cycles by passing only through states S2 and S4 to which it adds also state S1 at every 256 repetitions. Thus the typical time of the machine cycle is formed by two machine tacts and the speed of account accumulation may reach values close to $4{,}76 * 10^6$ [B/s]. The analog-digital converter which may ensure such speed, must have time for conversion shorter than 400 [ns].

2. Problems with synchronization

The control of an A/D-controller based on the system bus may be carried out only through software means. That's why the problems of the synchronization between the program (i.e. the processor) and the controller operation require explanation. In initial state the A/D-controller is inactive. Its activation with the purpose of data receiving from a outer real process is performed by the applied program in the needed moment. Further the program has to get into the algorithmic structure, shown on Fig.5.

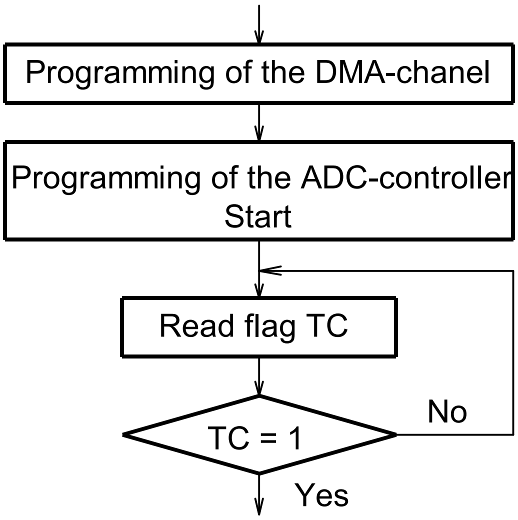
Programming of the DMA-chanel
Programming of the ADC-controller
Start
Read flag TC
TC = 1
No
Yes

Fig. 5

The condition block for controller examination performs its synchronization with the program. Regardless of the mode in which DMA-channel has carried out the data transfer, it is suitable that the A/D-controller be switched off by merely hardware means, through the signal. **TC** which the DMA-controller spreads through the system bus. Therefore, the synchronization could be achieved through reading of the status register connotation of the DMA-controller and through analysis of the value of the **TC** flag for the relevant DMA-channel.

The starting of the analog-digital conversion into A/D-controllers, commanded in single transfer mode could be reached after access permission from tact impulses to the converter. For that purpose through the **OUT** command in the program is being written initializing information in the relevant register of the A/D-controller to which corresponds the circuit shown on Fig.6.

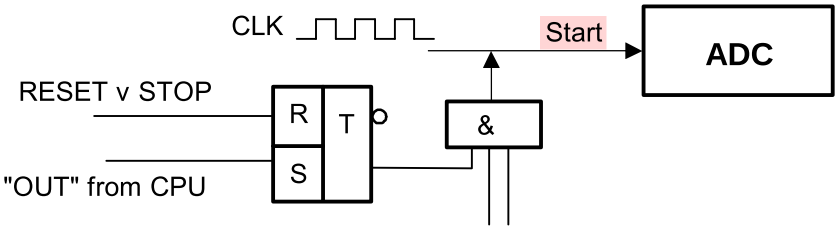

Fig. 6

The starting of the analog-digital conversion into A/D-controllers commanded in block transfer mode can not be performed by the means of the described static means. The starting impulses **I/O Read** in this mode (see Fig. 4) are being generated in the transfer process itself and if it’s not activated , then there is no way for those impulses to appear. That’s why the first starting impulse has to be formed by the program. This artificial forming of the first starting impulse can be achieved, for example, by a formal data reading from a register of the A/D-controller. The above-stated is being realized by the circuit shown on Fig. 7.

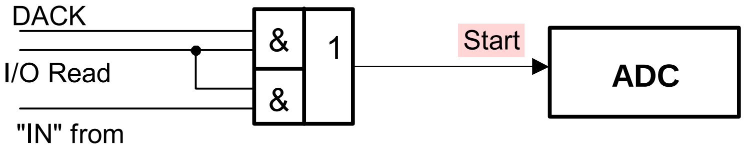

Fig. 7

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